

## SEMICONDUCTOR DEVICES AND METHODS FOR MANUFACTURING THE SAME

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Applicants hereby incorporate by reference Japanese Application No. 2000-132339, filed May 1, 2000 in its entirety. Applicants hereby incorporate by reference U.S. Application Serial No. \_\_\_\_\_, filed May 1, 2001, invented by Tatsuru Namatame and Kenji Yokoyama, having docket number 15.42/5850, in its entirety.

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### **Technical Field**

The present invention relates to semiconductor devices and methods for manufacturing the same, including semiconductor devices having an improved dielectric strength and methods for manufacturing the same.

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### **Related Art**

Presently, there is known a field effect transistor having a LOCOS (Local Oxidation Of Silicon) offset structure, which is a field effect transistor having an improved dielectric strength. A field effect transistor having a LOCOS offset structure is a transistor in which a LOCOS layer is provided between a gate dielectric layer and a drain region, wherein an offset impurity layer is formed below the LOCOS layer. For example, Japanese patent No. 2705106 and Japanese patent No. 2534508 describe field effect transistors having LOCOS offset structure.

It is noted that a field effect transistor having a LOCOS offset structure has a problem in which a bird's beak is formed at an end of the LOCOS such that the active region is narrowed.

### **Summary**

One embodiment relates to a semiconductor device including a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region.

A first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, and a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region. A first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the 5 second semi-recessed LOCOS layer.

Another embodiment relates to a method for manufacturing a semiconductor device including a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region. A first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region, and a second semi-recessed LOCOS layer is 10 provided between the gate dielectric layer and the source region. A first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer. The method includes forming a first recessed section in a region where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in a region where the second semi- 15 recessed LOCOS layer is to be formed. The method also includes implanting an impurity in a semiconductor substrate in the first recessed section and in the second recessed section. The method also includes thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section.

Another embodiment relates to a semiconductor device including first and second 20 field effect transistors, each including a gate dielectric layer and source and drain regions. The first and second field effect transistors also each include a first semi-recessed LOCOS layer positioned between the gate dielectric layer and the drain region, and a second semi-recessed LOCOS layer positioned between the gate dielectric layer and the source region. 25 The first and second field effect transistors also each include a first offset impurity layer below the first semi-recessed LOCOS layer, and a second offset impurity layer below the second semi-recessed LOCOS layer. The semiconductor device also includes an element isolation region located between the first and second field effect transistors.

### **Brief Description of the Drawings**

Embodiments of the invention are described with reference to the accompanying drawings which, for illustrative purposes, are schematic and not necessarily drawn to scale.

5 Fig. 1 schematically shows a semiconductor device in accordance with a first embodiment of the present invention.

Fig. 2 schematically shows a cross-sectional view in a manufacturing process in accordance with a second embodiment.

10 Fig. 3 schematically shows a cross-sectional view in the manufacturing process in accordance with the second embodiment.

Fig. 4 schematically shows a cross-sectional view in the manufacturing process in accordance with the second embodiment.

15 Fig. 5 schematically shows a cross-sectional view in the manufacturing process in accordance with the second embodiment.

Fig. 6 schematically shows a cross-sectional view in the manufacturing process in accordance with the second embodiment.

Fig. 7 schematically shows a cross-sectional view in the manufacturing process in accordance with the second embodiment.

20 Fig. 8 schematically shows a cross-sectional view in the manufacturing process in accordance with the second embodiment.

Fig. 9 schematically shows an enlarged cross-sectional view of a recessed section to describe a main portion in the method for manufacturing a semiconductor device in accordance with the third embodiment of the present invention.

### **Detailed Description**

25 Certain embodiments of the present invention relate to semiconductor devices having an improved dielectric strength and methods for manufacturing the same.

A semiconductor device in accordance with certain embodiments of the present invention may include a semiconductor having a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain

region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer.

5        In accordance with certain embodiments, for example, the following effects may be attained. The field effect transistor has a first semi-recessed LOCOS layer and a second semi-recessed LOCOS layer. Further, a first offset impurity layer and the second offset impurity layer are provided below the first semi-recessed LOCOS layer and the second semi-recessed LOCOS layer, respectively. Accordingly, the offset impurity layers can be  
10      made relatively deep with respect to the channel region compared to the case where semi-recessed LOCOS layers are not formed. As a result, when the field effect transistor is an ON state, deep depletion layers can be formed by the offset impurity layers. Consequently, the electric field adjacent the drain electrode is alleviated, to thereby increase the drain dielectric strength.

15        Also, in accordance with certain embodiments, the width of a bird's beak can be narrowed compared to the LOCOS layer. As a result, a miniaturization can be achieved compared to the LOCOS.

Also, in accordance with certain embodiments, the semiconductor device may preferably be used as a semiconductor device having a drain dielectric strength of 10 – 50 V.

20        Also, in particular, the semiconductor device may preferably be used as a high dielectric strength liquid crystal display (LCD) driver.

The semi-recessed LOCOS layer may have a thickness of 0.3 – 0.7  $\mu\text{m}$ , for example.

25        The semiconductor device may preferably have an element isolation region, and the element isolation region may preferably have a semi-recessed LOCOS structure. When the element isolation region has a semi-recessed LOCOS structure, the element isolation region may be formed in the same process in which the first and second semi-recessed LOCOS layers are formed. A channel stopper layer may be provided below the element isolation region.

30        A low concentration impurity layer having the same conductivity type as that of the drain region may preferably be provided around the drain region. By providing the low

concentration impurity layer, when the field effect transistor is an ON state, the region of the low concentration impurity layer becomes a depletion layer to thereby increase the drain dielectric strength.

A semiconductor device in accordance with certain embodiments of the present invention can be manufactured, for example, in the following manner.

A method for manufacturing a semiconductor device in accordance with certain embodiments of the present invention relates to a method for manufacturing a semiconductor device having a field effect transistor, the field effect transistor including a gate dielectric layer, a source region and a drain region, wherein a first semi-recessed

10 LOCOS layer is provided between the gate dielectric layer and the drain region, a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region, a first offset impurity layer is provided below the first semi-recessed LOCOS layer, and a second offset impurity layer is provided below the second semi-recessed LOCOS layer. The method for manufacturing a semiconductor device in accordance with certain

15 embodiments includes the steps of:

(a) forming a first recessed section in a region where the first semi-recessed LOCOS layer is to be formed, and forming a second recessed section in a region where the second semi-recessed LOCOS layer is to be formed

20 (b) implanting an impurity in a semiconductor substrate in the first recessed section and in the recessed section; and

(c) thermally oxidizing the semiconductor substrate to form the first semi-recessed LOCOS layer in the first recessed section and to form the second semi-recessed LOCOS layer in the second recessed section.

The method may further include the step (d) of forming an anti-oxidation layer 25 having a predetermined pattern, wherein the step (c) may preferably be conducted using the anti-oxidation layer formed on the semiconductor substrate as a mask.

As a result, the semiconductor substrate in a predetermined region can be securely 30 thermally oxidized. Also, in the step (b), when the impurity is implanted in the semiconductor substrate, the impurity is suppressed from being implanted in the semiconductor substrate that is covered by the anti-oxidation layer.

The anti-oxidation layer may preferably have a film thickness of 50 – 70 nm. When the film thickness of the anti-oxidation layer is 50nm or greater, when the impurity is implanted in the semiconductor substrate in the step (b), the impurity is prevented or inhibited from being implanted in the semiconductor substrate that is covered by the anti-oxidation layer.

Prior to the step (b), the step (e) of forming a protection layer over the semiconductor substrate in the first recessed section and the second recessed section may preferably be included. It is noted that the protection film is a film that suppresses damages to the semiconductor substrate when the impurity is implanted in the semiconductor substrate. By the inclusion of the step (e), damage to the semiconductor substrate in the first and second recessed sections can be suppressed.

The protection-layer may, for example, be a silicon oxide layer. The silicon oxide layer may be formed by a thermal oxidation method. By the thermal oxidation method, the silicon oxide layer can be securely formed over an exposed surface of the semiconductor substrate in the first recessed section and the second recessed section.

Also, when the protection film is formed, the step (f) of removing the protection film may preferably be included after the step (b). By the inclusion of the step (f), the film quality of the semi-recessed LOCOS layers thus obtained can be improved.

In the step (a), each of the first recessed section and the second recessed section may preferably be formed with a tapered configuration. As a result, in the step (b), the impurity can be readily implanted on side surfaces of the silicon substrate in the first and second recessed sections.

The first recessed section and the second recessed section may preferably have a tapered angle of 60 degrees or greater but preferably less than 90 degrees. As a result, in the step (b), the impurity can be readily implanted on side surfaces of the silicon substrate in the first and second recessed sections.

In the step (b), an implanting direction of the impurity may preferably traverse a normal line of a surface of the semiconductor substrate. As a result, in the step (b), the impurity can be readily implanted on side surfaces of the silicon substrate in the first and second recessed sections.

The implanting direction of the impurity and the normal line of the surface of the semiconductor substrate may preferably define an angle that is greater than zero degrees but preferably 45 degrees or less. As a result, in the step (b), the impurity can be readily implanted on side surfaces of the silicon substrate in the first and second recessed sections.

5 Preferred embodiments of the present invention are described below with reference to the accompanying figures.

A semiconductor device in accordance with a first embodiment of the present invention is described below. Fig. 1 schematically shows a cross-sectional view of a semiconductor device in accordance with the first embodiment of the present invention.

10 A semiconductor device 1000 includes element isolation regions 20. The element isolation regions 20 each have a semi-recessed LOCOS structure. A field effect transistor (herein below referred to as "transistor") 100 may be provided for each region defined by the element isolation regions 20.

15 The transistor 100 includes a gate dielectric layer 30, a source region 32, and a drain region 34. The source region 32 and the drain region 34 are each formed from an N<sup>+</sup>-type impurity diffusion layer formed in a P-type well in the case of an N-type transistor as an example; and are each formed from a P<sup>+</sup>-type diffusion layer formed in an N-type well in the case of a P-type transistor as an example.

20 First and second semi-recessed LOCOS layers 40 and 50 may be formed in a manner continuous with the gate dielectric layer 30. More concretely, the first semi-recessed LOCOS layer 40 is formed between the gate dielectric layer 30 and the drain region 34, and the second semi-recessed LOCOS layer 50 is formed between the gate dielectric layer 30 and the source region 32. The film thickness of the first and second semi-recessed LOCOS layers 40 and 50 may vary depending on the device designs, and may be, for example, 0.3 – 25 0.7 μm, and more preferably, 0.4 – 0.6 μm. First and second offset impurity layers 42 and 52 are formed below the first and second semi-recessed LOCOS layer 40 and 50, respectively. The first and second offset impurity layers 42 and 52 are each formed from an N-type impurity diffusion layer in the case of an N-type transistor as an example; and is formed from a P-type diffusion layer in the case of a P-type transistor as an example.

A channel stopper layer 60 may be formed in a central area of and below the element isolation region 20. The channel stopper layer 60 is formed from a P-type impurity diffusion layer in the case of an N-type transistor as an example; and is formed from an N-type diffusion layer in the case of a P-type transistor as an example.

5 Low concentration impurity layers 62 are formed below end sections of the element isolation region 20 adjacent to the drain regions 34. By the low concentration impurity layers 62, when the transistor is an ON state, the region of the low concentration impurity layers 62 becomes depletion layers such that the drain dielectric strength can be increased. The low concentration impurity layers 62 are each formed from an N-type impurity 10 diffusion layer in the case of an N-type transistor as an example; and formed from a P-type diffusion layer in the case of a P-type transistor as an example.

A contact region is formed in the semiconductor device 1000 to apply a voltage to the silicon substrate 10. The contact region is isolated from the source region or the drain region by the element isolation region. A channel stopper layer can be formed below the 15 element isolation region depending on the requirements.

An interlayer dielectric layer 70 is formed over the silicon substrate 10. Contact holes 72 are formed in specified regions of the interlayer dielectric layer 70. Wiring layers 74 are formed in the contact holes 72 and over the interlayer dielectric layer 70.

The semiconductor device 1000 in accordance with the first embodiment of the 20 present invention may have one or more of the effects described below.

(a) In the present embodiment, each of the transistors 100 has the semi-recessed LOCOS layers 40 and 50. Also, the offset impurity layers 42 and 52 are provided below the semi-recessed LOCOS layers 40 and 50. Therefore, the offset impurity layers 42 and 52 can be made relatively deep with respect to the channel region compared to the case where any 25 semi-recessed LOCOS layer is not formed. As a result, when the transistor is an ON state, a deep depletion layer can be formed by the offset impurity layers 42 and 52. Consequently, the electric field adjacent the drain electrode is alleviated, such that the drain dielectric strength is increased.

(b) Furthermore, the semiconductor device may preferably be used as a 30 semiconductor device having a drain dielectric strength of 10 – 50 V. Also, in particular, the

semiconductor device may preferably be used as a high dielectric strength liquid crystal display (LCD) driver.

A method for manufacturing a semiconductor device in accordance with a second embodiment of the present invention is described below. More particularly, taking an N-

5 type transistor as an example, a process for manufacturing a semiconductor device is described.

Figs. 2 – 8 schematically show cross-sectional views in a manufacturing process in accordance with the second embodiment.

(1) First, as shown in Fig. 2, a silicon oxide nitride layer 80 is formed over a silicon 10 substrate 10 by a CVD method. The silicon oxide nitride layer 80 has a film thickness of, for example, 8 to 12 nm. Then, a silicon nitride layer 82 is formed over the silicon oxide nitride layer 80 by a CVD method. The silicon nitride layer 82 may have any film thickness to the extent that it can prevent ions from being implanted in the silicon substrate 10 that is covered by the silicon nitride layer 82 in an ion implementation step to be described below.

15 The film thickness of the silicon nitride layer 82 may preferably be 50 – 70 nm, and more preferably 60 – 65 nm.

(2) Then, as shown in Fig. 3 (a), a first resist layer R1 having a predetermined pattern is formed over the silicon nitride layer 82. The first resist layer R1 has openings above regions where element isolation regions 20 and first and second semi-recessed LOCOS 20 layers 40 and 50 are to be formed.

Then, the silicon nitride layer 82, the silicon oxide nitride layer 80 and the silicon substrate 10 are etched using the first resist layer R1 as a mask. As a result, first through third recessed (or trench or concave) sections 84a, 84b and 84c are formed in regions where the element isolation regions 20 and the first and second semi-recessed LOCOS layers 40 25 and 50 are to be formed. Recessed section refers to an opening including, but not limited to, a concave opening or trench. The first recessed section 84a is formed in a region that becomes the first semi-recessed LOCOS layer 40, the second recessed section 84b is formed in a region that becomes the second semi-recessed LOCOS layer 50, and the third recessed section 84c is formed in a region that becomes the element isolation region 20. It is noted 30 that Fig. 3 (b) schematically shows an enlarged cross-sectional view of the first recessed

section 84a of Fig. 3 (a). The width W10 of the first recessed section 84a may differ depending on the dielectric strength and characteristics of the device, and may be, for example, 0.3 – 5.0  $\mu\text{m}$ , and more preferably, 0.5 – 2.0  $\mu\text{m}$ . The depth D10 of the first recessed section 84a may differ depending on the dielectric strength and characteristics of the device, and may be, for example, 0.05 – 0.15  $\mu\text{m}$ , and more preferably, 0.08 – 0.1  $\mu\text{m}$ .  
5 The width and the depth of the second recessed section 84b may be the same as those of the first recessed section 84a. The depth of the third recessed section 84c may be the same as that of the first recessed section 84a. Then, the first resist layer R1 is removed.

(3) Then, as shown in Fig. 4 (a), a silicon oxide layer 90 is formed over an exposed 10 surface of the silicon substrate 10 by a thermal oxidation method. It is noted that Fig. 4 (b) schematically shows an enlarged cross-sectional view of the first recessed section 84a of Fig. 4 (a). It is noted that the silicon oxide layer 90 can be formed by a CVD method. The film thickness of the silicon oxide layer 90 may be, for example, 5.0 – 10 nm, and more preferably, 6.0 – 7.0 nm.

(4) Then, as shown in Fig. 5 (a), a second resist layer R2 having a predetermined 15 pattern is formed. The second resist layer R2 has openings provided above the first recessed sections 84a and the second recessed sections 84b, and end sections of the third recessed sections 84c. More concretely, the openings are provided above regions where the first and second semi-recessed LOCOS layers 40 and 50 and the low concentration impurity layers 62 20 are to be formed.

Then, N-type ions 92a are implanted in the silicon substrate 10 using the second resist layer R2 as a mask. As a result, N-type impurity diffusion layers 92 are formed in the first through third recessed sections 84a, 84b and 84c. In succeeding steps, the N-type 25 impurity diffusion layers 92 in the first and second recessed sections 84a and 84b become first and second offset impurity layers 42 and 52, respectively. Also, the N-type impurity diffusion layers 92 in the third recessed sections 84c become low concentration impurity layers 62.

It is noted that Fig. 5 (b) schematically shows an enlarged cross-sectional view of the first recessed section 84a of Fig. 5 (a). Because the silicon oxide layer 90 is formed, damage 30 by the ion implantation to the silicon substrate 10 in the first though third recessed sections

84a, 84b and 84c are suppressed. As a result, crystal lattices of the silicon substrate 10 are severed such that the formation of electrical current paths is suppressed. The N-type ions 92a may be, for example, phosphorous ions. The ion acceleration voltage may vary depending on the dielectric strength and characteristics of the device, and may be, for

5 example, 10 – 50 keV, and more preferably 20 – 25 keV. The dose may vary depending on the dielectric strength and characteristics of the device, and may be, for example, 1.0E + 13 to 1.5E + 14 cm<sup>-2</sup>, and more preferably, 3.0E + 13 to 5.0E + 13 cm<sup>-2</sup>. The ion implantation angle (an angle defined between a normal line L1 of the surface of the semiconductor substrate and a direction in which the ions are implanted)  $\theta$  is not particularly limited, and  
10 may be, for example, 0 – 45 degrees, and more preferably, greater than zero (0) degrees but 45 degrees or less, and even more preferably, between 5 degrees and 20 degrees. When the ion implantation angle  $\theta$  is greater than zero (0) degrees but 45 degrees or smaller, the ions can be securely implanted in the side surfaces of the silicon substrate 10 in the recessed sections 84a, 84b and 84c. Then, the second resist layer R2 is removed.

15 (5) Then, as shown in Fig. 6, a third resist layer R3 having a predetermined pattern is formed. The third resist layer R3 has an opening provided in a central section of the third recessed section 84c. More concretely, the third resist layer R3 has the opening provided above a region where the channel stopper layer 60 is to be formed.

Then, P-type ions 94a are implanted in the silicon substrate 10 using the third resist 20 layer R3 as a mask. As a result, P-type impurity diffusion layers 94 are formed in the third recessed sections 84c. In succeeding steps, the P-type impurity diffusion layers 94 become channel stopper layers 60. The P-type ions 94a may be, for example, boron ions. The ion acceleration voltage may vary depending on the dielectric strength and characteristics of the device, and may be, for example, 5 – 10 keV, and more preferably 7 – 8 keV. The dose may  
25 vary depending on the dielectric strength and characteristics of the device, and may be, for example, 1.0E + 13 to 1.5E + 14 cm<sup>-2</sup>, and more preferably, 3.0E + 13 to 1.0E + 14 cm<sup>-2</sup>. Then, the third resist layer R3 is removed.

(6) Then, as shown in Fig. 7 (a), the silicon oxide layer 90 is removed. It is noted that Fig. 7 (b) schematically shows an enlarged cross-sectional view of the first recessed

section 84a of Fig. 7 (a). It is noted that the silicon oxide layer 90 may not have to be removed if it does not adversely affect the characteristics of the device.

Then, the silicon substrate 10 is thermally oxidized using the silicon nitride layer 82 as an anti-oxidation layer. As a result, as shown in Fig. 8, the element isolation regions 20 and the first and second semi-recessed LOCOS layers 40 and 50 are formed. In this thermal oxidation step, the ions implanted in the silicon substrate 10 in the first and second recessed sections 84a and 84b are defused (driven in), such that first and second offset impurity layers 42 and 52 are formed. Also, at the same time, the ions implanted in the silicon substrate 10 in the third recessed sections 84c are defused (driven in), such that channel stopper layers 60 and low concentration impurity layers 62 are formed.

Then, the silicon nitride layer 82 and silicon oxide nitride layer 80 are removed. Then, the surface of the silicon substrate 10 is thermally oxidized to form gate dielectric layers 30.

(7) Next, as shown in Fig. 1, a conductive polysilicon layer is deposited over the wafer including the LOCOS layers 20. Next, by conducting photolithography and etching, gate electrodes 36 are formed over the gate dielectric layers 30. Then, sidewalls may be formed on the sides of the gate electrodes 36 depending on the requirements.

Then, phosphorus ions are implanted using the gate electrodes 36 and the first and second semi-recessed LOCOS layers 40 and 50 as a mask to form source/drain regions 32, 34 of an N-channel transistor.

Then, an interlayer dielectric layer 70 is deposited over the wafer including the gate electrodes 36. By conducting photolithography and etching, contact holes 72 are formed in the interlayer dielectric layer 70.

Then, a conduction layer formed from, for example, an aluminum alloy, copper, or the like is deposited in the contact holes 72 and over the interlayer dielectric layer 70; and the conduction layer is patterned to form wiring layers 74.

The method for manufacturing the semiconductor device in accordance with the second embodiment of the present invention may have one or more of the effects described below.

(a) In accordance with the present embodiment, when implanting ions in the recessed sections 84a, 84b and 84c, the silicon oxide layer 90 is formed over the surface of the silicon substrate 10 in the recessed sections 84a, 84b and 84c. As a result, damages by the ion implantation to the silicon substrate 10 in the recessed sections 84a, 84b and 84c are suppressed. As a result, crystal lattices of the silicon substrate 10 are severed such that the formation of electrical current paths is suppressed.

(b) In the step of implanting ions in the silicon substrate 10 in the first and second recessed sections 84a and 84b, when the ion implantation angle  $\theta$  is greater than zero (0) degrees but 45 degrees or less, the following effects may be achieved. Namely, when the ion implantation angle  $\theta$  is greater than zero (0) degrees but 45 degrees or less, the ions can be securely implanted on sides of the silicon substrate 10 in the first and second recessed sections 84a and 84b. As a result, the first and second offset impurity layers 42, 52 can be securely formed on the sides of the first and second semi-recessed LOCOS layers 40 and 50.

It is noted that, P-type transistors can be manufactured in parallel with the manufacturing of the N-type transistors. For example, P-type transistors can be manufactured in parallel with the manufacturing of the N-type transistors in the following manner.

(A) Recessed sections in regions where offset impurity layers of the P-type transistors are to be formed may be formed at the same time when the above-described recessed sections are formed in the forming step (2). (B) The step of implanting P-type ions to form the offset impurity layers of the P-type transistors may be conducted at the same time when the step (5) to form the above-described channel stopper layers is conducted.

Next, a method for manufacturing a semiconductor device in accordance with a third embodiment of the present invention is described below. Fig. 9 schematically shows an enlarged cross-sectional view of a recessed section to describe a main portion in the method for manufacturing a semiconductor device in accordance with the third embodiment of the present invention.

The third embodiment is different from the second embodiment in the method of forming recessed sections. The third embodiment is the same as the second embodiment

except the method of forming recessed sections, and therefore a detailed description thereof is omitted.

In the third embodiment, as shown in Fig. 9, the silicon substrate 10 is etched in a manner that the first and second recessed sections 84a and 84b each have a tapered configuration. The taper angle  $\alpha$  of the recessed section is less than 90 degrees, more preferably, 60 degrees or greater but less than 90 degrees, and even more preferably between 70 and 80 degrees. An etching method for forming the recessed sections may not particularly be limited as long as the method can provide the first and second recessed sections 84a with tapered shapes. More concretely, the silicon substrate 10 may be etched by an etching apparatus having parallel plate electrodes in the following manner as an example.

First, the silicon substrate 10 is disposed over the parallel plate lower electrode. Power of, for example, 200 W may be applied between the electrodes to etch the silicon substrate 10. As a concrete condition, the etching is conducted under a vacuum having a pressure of, for example 700 mTorr. An etching gas to be used in the etching may be a gas including, for example, CHF<sub>3</sub>, CF<sub>4</sub>, Ar, O<sub>2</sub>, and the quantity ratio of these gases may be, for example, 10/70/800/4 sccm (= CHF<sub>3</sub> / CF<sub>4</sub> / Ar / O<sub>2</sub>).

The method for manufacturing the semiconductor device in accordance with the third embodiment of the present invention may include one or more of the effects described below.

(a) The third embodiment may provide a similar effect as the effect (a) of the second embodiment.

(b) In the third embodiment, the recessed sections 84a and 84b are formed to have tapered configurations (the taper angle  $\alpha$  is less than 90 degree). As a result, in a step of implanting ions in the silicon substrate 10 in the recessed sections 84a and 84b, the ions can be securely implanted in the sides of the second substrate 10. As a result, the first and second offset impurity layers 42 and 52 can be securely formed on the sides of the first and second semi-recessed LOCOS layers 40 and 50.

The present invention is not limited to the embodiments described above, and a variety of other embodiments can be made within the scope of the subject matter of the invention.